ABSTRACT OF THE DISCLOSURE

A semiconductor memory device comprises a memory cell array, a decoder unit selecting a word line of the memory cell array, a first dummy cell array connected to a first dummy bit line and disposed with the memory cell array at a first location away from the decoder unit along the word line, a second dummy cell array connected to second dummy bit lines and disposed with the memory cell array at a second location away from the decoder unit along the word line, the second location being farther from the decoder unit than the first location, and a timing control unit determining timing of activation and deactivation of an internal control signal.